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AN INTERCONNECTION NETWORK FOR A FIELD PROGRAMMABLE GATE ARRAY

CROSS-REFERENCES TO RELATED APPLICATIONS

This patent application claims priority from Provisional Patent Application No. 60/223,047, filed August 4, 2000, and is a continuation of U.S. Patent Application No. 09/923,294, filed August 3, 2001 (is now a U.S. Patent 6,693,456), all of which are hereby incorporated by reference.

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BACKGROUND OF THE INVENTION

The present invention relates to integrated circuit interconnections and, in particular, to the interconnection architecture of FPGA (Field Programmable Gate Array) integrated circuits.

FPGAs are integrated circuits whose functionalities are designated by the users of the FPGA. The user programs the FPGA (hence the term, "field programmable") to perform the functions desired by the user.

A very significant portion of an FPGA's design is the integrated circuit's interconnection network between the logic cells or blocks, which perform the functions of the FPGA. Heretofore, the current practice for designing an FPGA interconnection architecture has been empirical and on an *ad hoc* basis. The goal of the FPGA designer has been to create an interconnect structure which is sufficiently flexible to implement the required wiring for any circuit design intended for the FPGA, and yet occupies a minimal amount of area of the integrated circuit and with a minimal amount of transmission delay. In today's FPGA products, the interconnect network typically occupies about 90% of the chip area and the actual logic cells occupy only about 5% of the chip. In other words, most of the area of the integrated circuit is not dedicated to the circuits performing desired functions of the FPGA, but rather to the interconnections between those circuits.

Furthermore, the current practice for designing FPGA interconnects is empirical and on an *ad hoc* basis. The users of these FPGA products spend most of their design time trying to make their circuits route to obtain the desired functions and to meet the timing constraints. The rule of thumb is to only utilize 50% of the available logic cells in order to guarantee they can all be routed through the interconnect network. If the timing